AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for minimizing clock feedthrough effect when switching off a switched capacitor circuit, comprising:

providing a plurality of differently sized positive side switch elements for selectively connecting a positive side first node to a positive side second node depending upon a control signal applied to a first control terminal of each of the switch elements, wherein the positive side first node is connected to a positive side capacitor; and

when switching the switched capacitor circuit to an off state, sequencing the control signals such that the positive side switch elements are switched offsequentially.

2. (original) The method of claim 1, wherein the plurality of positive side switch elements is a plurality of differently sized positive side switch elements for selectively connecting a positive side first node to a positive side second node depending upon a control signal applied to a first control terminal of each of the switch elements; and

when switching the switched capacitor circuit to an off state, sequencing the control signals such that the positive side switch elements are switched off in decreasing order based on switch size, whereby the largest switch element is switched off first and the smallest switch element is switched off last.

3. (original) The method of claim 2, further comprising when switching the switched capacitor circuit to an off state, providing a means for making the smallest positive

side switch element gradually switch off.

4. (original) The method of claim 3, wherein each switch element is a transistor and the means for making the smallest positive side switch element gradually switch off comprises a low-pass filter connected to the first control terminal of the smallest positive side switch element.

5. (original) The method of claim 3, wherein the positive side second node is ground and the switch elements comprise NMOS transistors.

6. (original) The method of claim 2, further comprising:

for each switch element in the plurality of differently sized positive side switch elements, providing a corresponding negative side switch element having substantially the same size as the positive side switch element for selectively connecting a negative side first node to a negative side second node depending upon the control signal applied to the first control terminal of the positive side switch element, wherein the negative side first node is connected to a negative side capacitor; and

7. (original) The method of claim 6, further comprising:

providing a center switch element for selectively connecting the positive side first node to the negative side first node depending upon a center control signal applied to the third control terminal of the center switch element; and

when switching the switched capacitor circuit to an off state, sequencing the control signals such that the center switch element is switched off first and then the positive

side switch elements and the corresponding negative side switch elements are switched off in decreasing order based on size.

8. (original) The method of claim 6, further comprising when switching the switched capacitor circuit to an off state, providing a means for making the smallest positive side switch element and its corresponding negative side switch element gradually switch off.

9. (original) The method of claim 8, wherein each switch element is a transistor and the means for making the smallest positive side switch element and its matched negative side switch element gradually switch off comprises a low-pass filter connected to the first control terminal of the smallest positive side switch element and its matched negative side switch element.

10. (original) The method of claim 8, wherein the positive side second node is ground, the negative side second node is ground, and the switch elements comprise NMOS transistors.

11. (original) A switched capacitor circuit capable of minimizing clock feedthrough effect, comprising:

a plurality of positive side switch elements for selectively connecting a positive side first node to a positive side second node depending upon a control signal applied to a first control terminal of each of the switch elements, wherein the positive side first node is connected to a positive side capacitor; and

a sequence controller electrically connected to the positive side switch elements for generating the control signals to switch off the differently sized positive side switch

elements sequentially.

12. (original) The switched capacitor circuit of claim 11, wherein:

the plurality of positive side switch elements is a plurality of differently sized positive side switch elements for selectively connecting a positive side first node to a positive side second node depending upon a control signal applied to a first control terminal of each of the switch elements; and

the sequence controller electrically connected to the differently sized positive side switch elements is for generating the control signals to switch off the differently sized positive side switch elements in decreasing order based on switch size.

13. (original) The switched capacitor circuit of claim 12, further comprising a means for making the smallest positive side switch element gradually switch off.

14. (original) The switched capacitor circuit of claim 13, wherein each switch element is a transistor and the means for making the smallest switch element gradually switch off comprises a low-pass filter connected to the first control terminal of the smallest positive side switch element.

15. (original) The switched capacitor circuit of claim 14, wherein the second positive side node is ground and the positive side switch elements comprise NMOS transistors.

16. (original) The switched capacitor circuit of claim 12, further comprising:

for each switch element in the plurality of differently sized positive side switch

elements, a corresponding negative side switch element having substantially the same size as the positive side switch element for selectively connecting a negative side first node to a negative side second node depending upon the control signal applied to the first control terminal of the positive side switch element, wherein the negative side first node is connected to a negative side capacitor.

17. (original) The switched capacitor circuit of claim 16, further comprising:

a center switch element for selectively connecting the positive side first node to the negative side first node depending upon a center control signal;

wherein the sequence controller is further connected to the center switch element and generates a center control signal, and the sequence controller switches off the center switch element first and then the positive side switch elements are switched off in decreasing order based on switch size.

18. (original) The switched capacitor circuit of claim 16, further comprising a means for making the smallest positive side switch element and its corresponding negative side switch element gradually switch off.

19. (original) The switched capacitor circuit of claim 18, wherein each switch element is a transistor and the means for making the smallest positive side switch element and its matched negative side switch element gradually switch off comprises a lowpass filter connected to the first control terminal of the smallest positive side switch element and its corresponding negative side switch element.

20. (original) The switched capacitor circuit of claim 18, wherein the positive side second node is ground, the negative side second node is ground, and thepositive

side switch elements, the negative side switch elements, and the center switch element comprise NMOS transistors.